

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application No.: 10/821,371

Filed: April 9, 2004

Inventor(s):

Landin et al.

§ Examiner: Patel, K. M.

§ Group/Art Unit: 2188

§ Atty. Dkt. No: 5181-25901

§ Confirm No. 1212

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VII. ARGUMENT

First Ground of Rejection:

Claims 7, 18, and 22

Appellant maintains the arguments presented in the Appeal Brief dated June 23, 2008. Appellant has added additional arguments below to further clarify why the Appellant's claims patentably distinguish over the cited art.

In the response to arguments section of the Examiner's Answer, the Examiner asserts (*See page 8, section 10 of the Examiner's Answer dated July 9, 2008*) “[a]ppellant argues: Rowlands-1 is merely disclosing that the memory bridge 32 can request, via coherency commands (probes), ownership from other nodes and the probes referred to by the Examiner are sent out of the node to other nodes and not within the node to the processors.” The Examiner then substantively argues why what Appellant stated is incorrect. However, Appellant also stated “[i]n other words, the memory bridge 32 does not initiate a different kind of command such as a “proxy packet” internally on the interconnect 22 in response to receiving a coherency command from another node via the interfaces 30. Appellant contends (and argues further below) that the commands on the interconnect 22 are the same irrespective of whether they are remote or local commands.”

Appellant notes Rowlands1 appears to use the phrase “coherency commands” interchangeably at times. For example, as previously presented in the Appeal Brief, Rowlands1 discloses (*See Rowlands1 Col. 5, lines 5-12*) (emphasis added) “[a]s used herein, coherency commands include any communications between nodes that are used to maintain coherency between nodes. The commands may include read or write requests initiated by a node to fetch or update a cache block belonging to another node, probes to invalidate cached copies of cache blocks in remote nodes (and possibly to return a modified copy of the cache block to the home node), responses to probe commands, fills which transfer data, etc.

As previously argued in the Appeal Brief, Appellant's claim 7 recites a multi-node system comprising in pertinent part

an inter-node network configured to convey coherency messages between the interface in the node and an additional interface in an additional node, wherein the additional interface is configured to send a coherency message requesting a read access right to a coherency unit on the inter-node network, wherein a given active device of the plurality of active devices has an ownership responsibility for the coherency unit;

wherein the interface is configured to respond to the coherency message by sending a proxy address packet on the address network;

wherein a different active device of the plurality of active devices is configured to request a read access right to another coherency unit by sending an address packet on the address network;

wherein the given active device of the plurality of active devices has an ownership responsibility for the another coherency unit, wherein the given active device is configured to not transition the ownership responsibility for the another coherency unit in response to the address packet and to transition the ownership responsibility for the coherency unit in response to the proxy address packet. (Emphasis added)

Rowlands1 also discloses (See Rowlands1 Col. 5, lines 47-62) (emphasis added) “[f]or example, in one embodiment, if a transaction on the interconnect 22 (e.g. a transaction issued by the processors 12 A- 12 N) accesses a cache block that is remote to the node 10 (i.e. the cache block is part of the memory coupled to a different node) and the node 10 does not have sufficient ownership to perform the transaction, the memory bridge 32 may issue one or more coherency commands to the other nodes to obtain the ownership (and a copy of the cache block, in some cases). Similarly, if the transaction accesses a local cache block but one or more other nodes have a copy of the cache block, the memory bridge 32 may issue coherency commands to the other nodes. Still further, the memory bridge 32 may receive coherency commands from other nodes, and may perform transactions on the interconnect 22 to effect the coherency commands.

From the foregoing, Appellant submits Rowlands1 is merely disclosing that the memory bridge 32 can request, via coherency commands (of whatever kind they are),

ownership from other nodes. In addition Rowlands1 also discloses performing *transactions* on the interconnect to effect the coherency commands from other nodes.

Thus it is clear that the probes and/or any other coherency messages referred to by the Examiner are sent OUT of the node to other nodes and *transactions* (of an unknown variety) are used on the interconnect within the node to/from the processors.

In other words, Rowlands1 does not disclose the memory bridge 32 initiating a transaction such as a “proxy packet” internally on the interconnect 22 in response to receiving a coherency command from another node, that is different than a transaction that a processor would initiate on the interconnect 22. Appellant contends that Rowlands1 only discloses *transactions* on the interconnect 22 and is silent on the form of those transactions, irrespective of whether they were initiated remotely or locally. Thus, Appellant submits the probes referred to by the Examiner **cannot** be the proxy packets recited in Appellant’s claims.

Appellant submits neither Rowlands2 nor Chen is relied upon, nor do they teach or suggest the above limitations. Thus Appellant submits none of the cited references teach or suggest “wherein the interface is configured to respond to the coherency message by sending a *proxy address packet on the address network*” or “wherein a different active device of the plurality of active devices is configured to request a read access right to another coherency unit by sending *an address packet on the address network*” or “wherein the given active device of the plurality of active devices has an ownership responsibility for the another coherency unit, wherein the given active device is configured to not transition the ownership responsibility for the another coherency unit in response to the address packet and to transition the ownership responsibility for the coherency unit in response to the proxy address packet,” as recited in claim 7.

Accordingly, Appellant submits none of the references taken either singly or in combination, teaches or suggests the combination of features recited in Appellant's claim 7.

Claims 18, and 22 recite features that are similar to features recited in claim 7. Accordingly, for at least the above stated reasons, Appellant submits that the rejection of claims 7, 18, and 22 is in error and requests reversal of the rejection. The rejections of claims 8-13, and 15 (dependent from claim 7), claims 19-20 (dependent from claim 18), and claims 23-28 (dependent from claim 22) are similarly in error for at least the above stated reasons, and reversal of the rejection is requested. Each of claims 8-15, 19-21, and 23-29 recite additional combinations of features not taught or suggested in the cited art.

CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 7-29 is erroneous, and reversal of his decision is respectfully requested.

The Commissioner is authorized to charge any fees and/or credit any overpayments that may be due to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-25901/SJC.

Respectfully submitted,

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